LTES - Bug #27

Tic Timer "CMD" Mode to "OSC" Mode transition delay

06/21/2019 12:46 PM - Greg Mathis

Status:	Closed	**Start date:**	06/21/2019
Priority:	Normal	**Due date:**	
Assignee:	Jennifer Lazbin	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:		**Spent time:**	0.00 hour

Description

When LTES is receiving Time Update commands, with no 1 PPS signal, the Tic Timer Mode will become "CMD". However, if the Time Update commands are less frequent than 1 every 2 seconds, Tic Timer Mode will become "OSC". I think that was nominal for EMIRS. But for LTES, requirement "L-TES_ICD-183" states nominal time update interval is every 5 seconds. So I'm thinking the Tic Timer Mode should take longer (6 seconds?) to transition to "OSC" mode.

History

#1 - 06/28/2019 08:21 AM - Greg Mathis

- Status changed from New to Closed

Fixed with FPGA version 3.12